BD249C

NPN High-Power Transistor

NPN high−power transistors are for general−purpose power amplifier and switching applications.

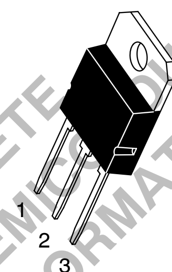
Features

- ESD Ratings: Machine Model, C; > 400 V
  Human Body Model, 3B; > 8000 V
- Epoxy Meets UL 94 V−0 @ 0.125
- Pb−Free Package is Available*

ON Semiconductor®

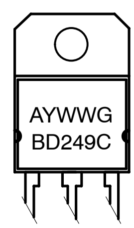
http://onsemi.com

25 AMP, 100 VOLT, 125 WATT NPN SILICON POWER TRANSISTOR



TO−218 CASE 340D STYLE 1

MARKING DIAGRAM



BD249C	=	Device Code
A	=	Assembly Location
Y	=	Year
WW	=	Work Week
G	=	Pb−Free Package

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	100	Vdc
Collector − Base Voltage	V_{CBO}	100	Vdc
Emitter − Base Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous Peak (Note 1)	I_C	25 40	Adc Apk
Base Current − Continuous	I_B	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1.0	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C
Unclamped Inductive Load	E_{SB}	90	mJ

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	35.7	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ORDERING INFORMATION

Device	Package	Shipping
BD249C	TO−218	30 Units/Rail
BD249CG	TO−218 (Pb−Free)	30 Units/Rail

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

August, 2006 − Rev. 2

Publication Order Number:
BD249C/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 30 mA, I_B = 0)	$V_{CEO(sus)}$	100	–	V
Collector−Emitter Cutoff Current (V_{CE} = 60 V, I_B = 0)	I_{CEO}	–	1.0	mA
Collector−Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)	I_{CES}	–	0.7	mA
Emitter−Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)	I_{EBO}	–	1.0	mA
ON CHARACTERISTICS (Note 1)				
DC Current Gain	h_{FE}			–
(I_C = 1.5 A, V_{CE} = 4.0 V)		25	–	
(I_C = 15 A, V_{CE} = 4.0 V)		10	–	
(I_C = 25 A, V_{CE} = 4.0 V)		5.0	–	
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$			V
(I_C = 15 A, I_B = 1.5 A)		–	1.8	
(I_C = 25 A, I_B = 5.0 A)		–	4.0	
Base−Emitter On Voltage	$V_{BE(on)}$			V
(I_C = 15 A, V_{CE} = 4.0 V)		–	2.0	
(I_C = 25 A, V_{CE} = 4.0 V)		–	4.0	
DYNAMIC CHARACTERISTICS				
Small−Signal Current Gain (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 kHz)	h_{fe}	25	–	–
Current−Gain — Bandwidth Product (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 MHz)	f_T	3.0	–	MHz

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

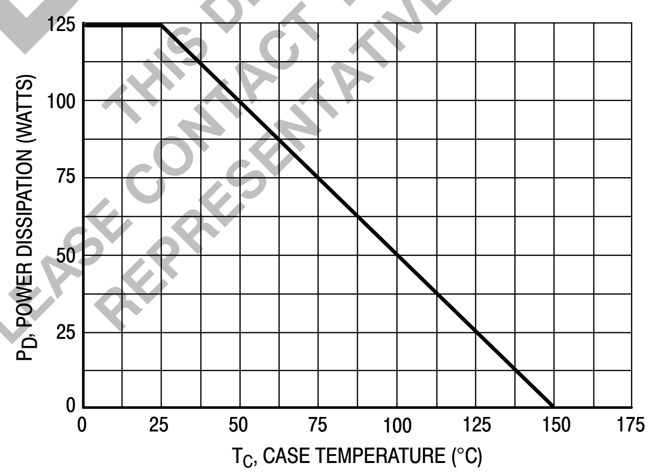


Figure 1. Power Derating

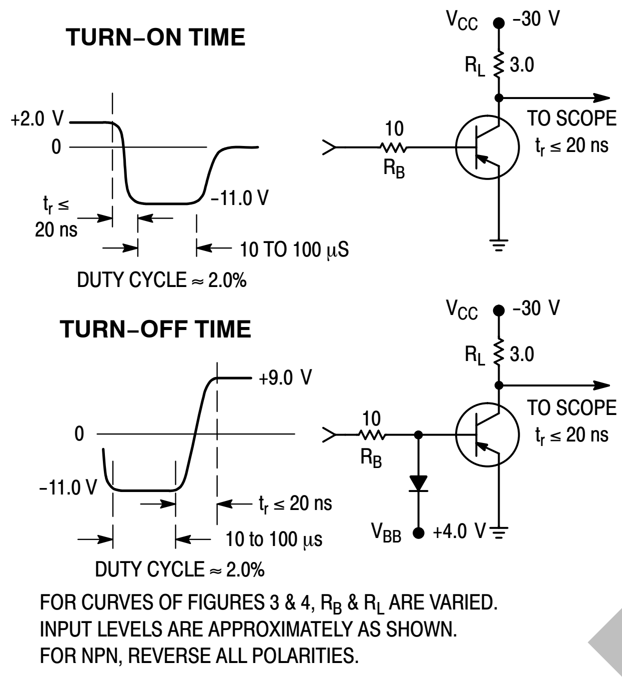


Figure 2. Switching Time Equivalent Test Circuits

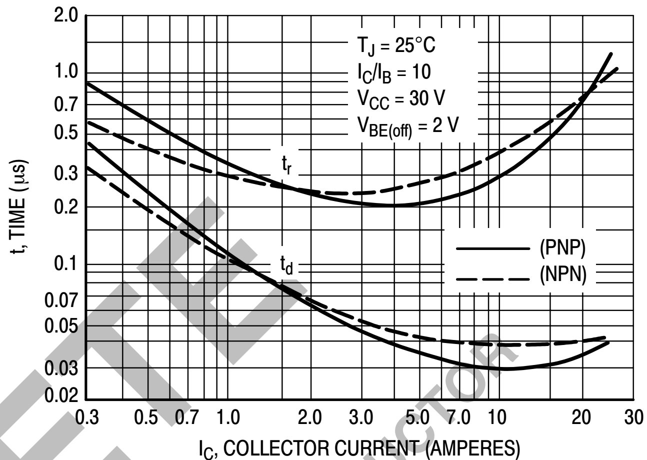


Figure 3. Turn−On Time

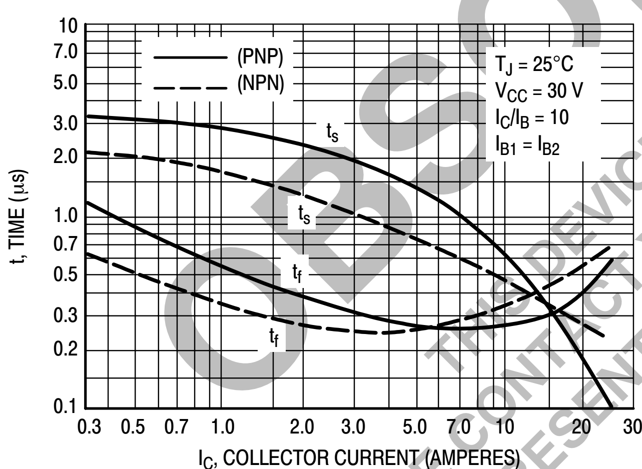


Figure 4. Turn−Off Time

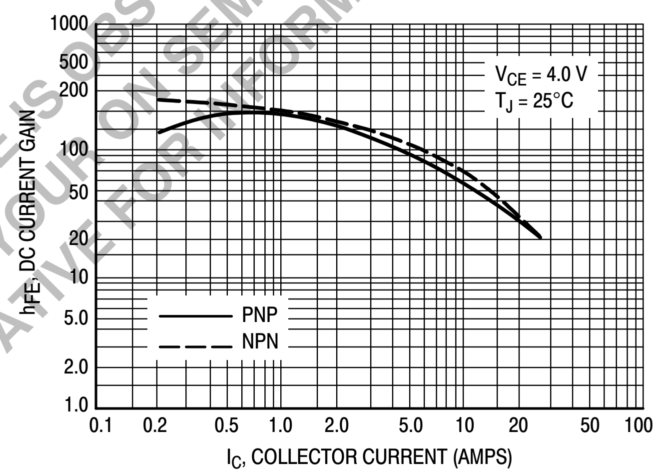


Figure 5. DC Current Gain

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives RBSOA characteristics.

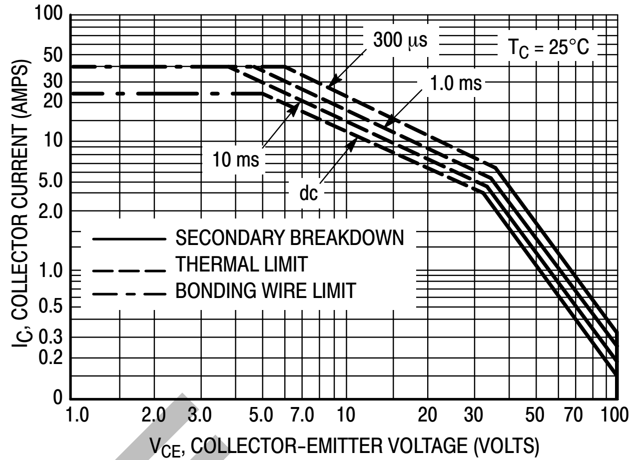


Figure 6. Maximum Rated Forward Bias Safe Operating Area

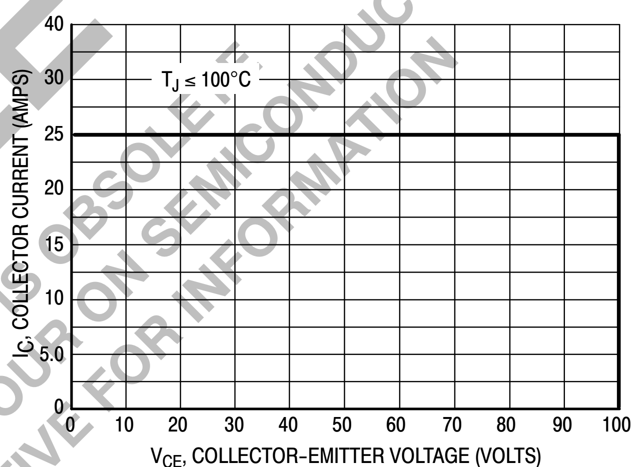
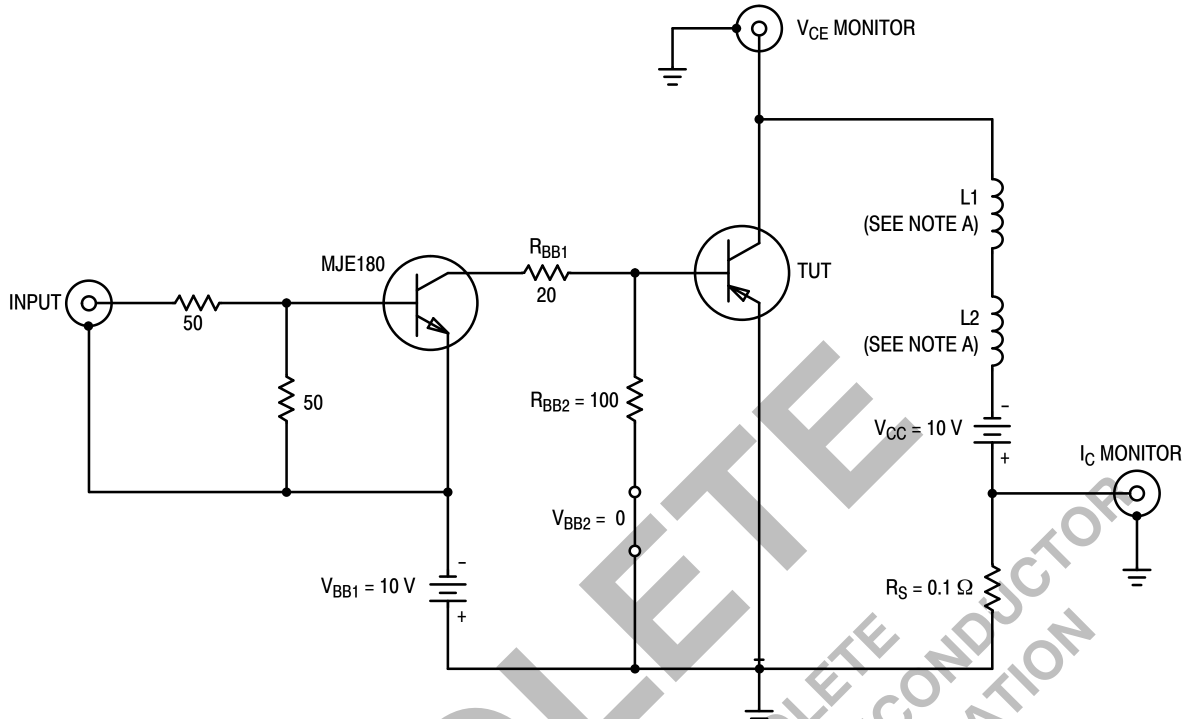
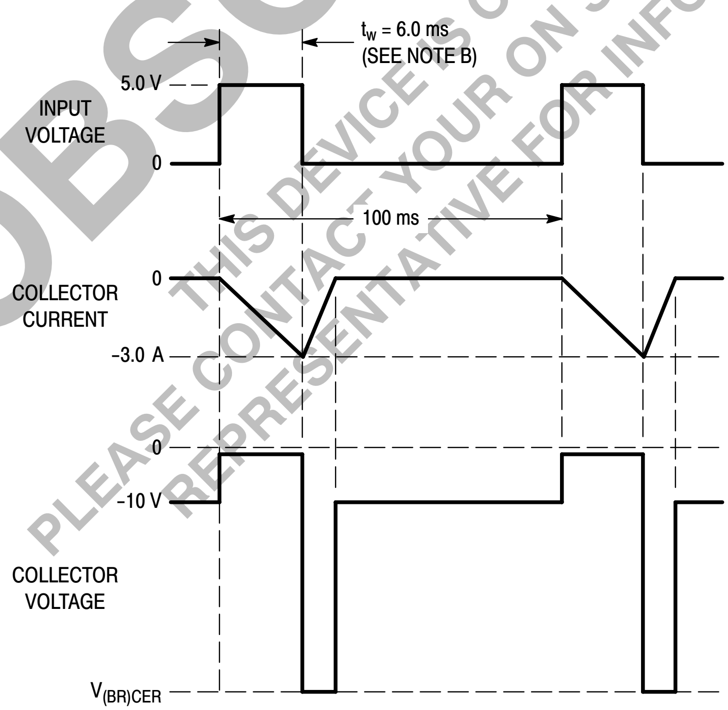


Figure 7. Maximum Rated Forward Bias Safe Operating Area

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



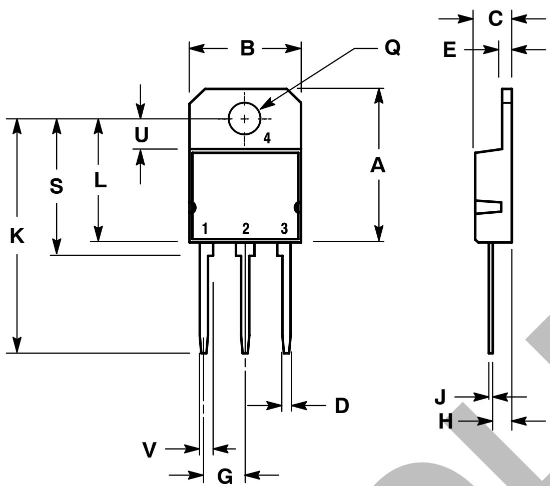
NOTES:

A. L1 and L2 are 10 mH, 0.11 Ω, Chicago Standard Transformer Corporation C−2688, or equivalent.
B. Input pulse width is increased until I_{CM} = −3.0 A.
C. For NPN, reverse all polarities.

Figure 8. Inductive Load Switching

PACKAGE DIMENSIONS

TO−218
CASE 340D−02
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	---	16.20	---	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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