COS/MOS INTEGRATED CIRCUIT

HCC/HCF 40174B

PRELIMINARY DATA

HEX "D" - TYPE FLIP-FLOP

- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 40174B** (extended temperature range) and **HCF 40174B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package, and ceramic flat package.
The **HCC/HCF 40174B** consists of six identical 'D'-type flip-flops having independent DATA inputs. The CLOCK and $\overline{\text{CLEAR}}$ inputs are common to all six units. Data is transferred to the Q outputs on the positive-going transition of the clock pulse. All six flip-flops are simultaneously reset by a low level on the $\overline{\text{CLEAR}}$ input.

ABSOLUTE MAXIMUM RATINGS *

V_{DD} **	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	±10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature range: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

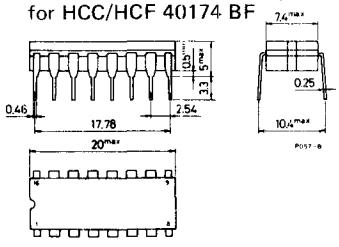
** All voltages are with respect to V_{SS} (GND).

ORDERING NUMBERS:

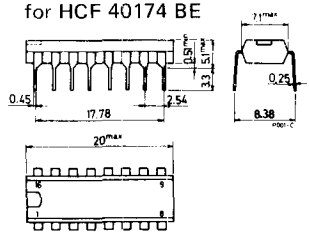
HCC 40174 BD for dual in-line ceramic package
HCC 40174 BF for dual in-line ceramic package, frit seal
HCC 40174 BK for ceramic flat package
HCF 40174 BE for dual in-line plastic package
HCF 40174 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

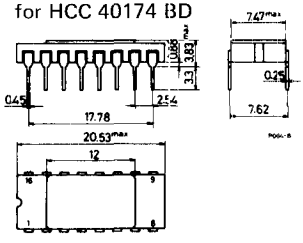
Dual in-line ceramic package for HCC/HCF 40174 BF



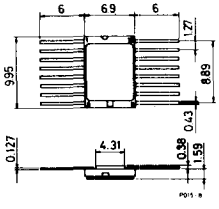
Dual in-line plastic package for HCF 40174 BE



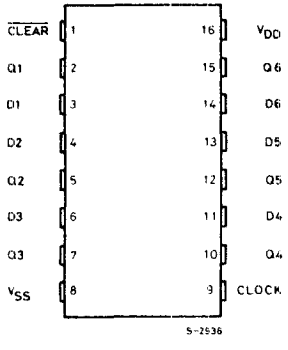
Dual in-line ceramic package for HCC 40174 BD



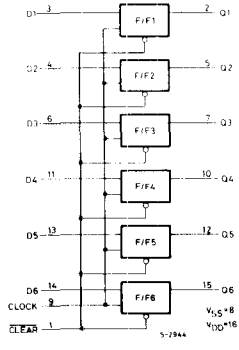
Ceramic flat package for HCC 40174 BK



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

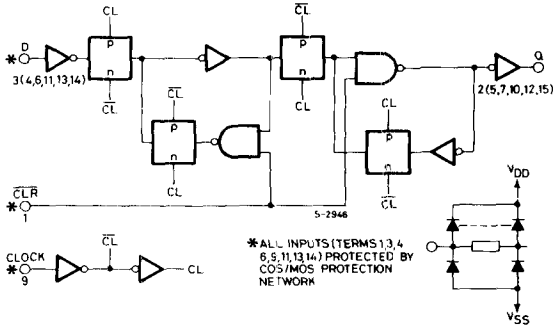


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature range: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM AND TRUTH TABLE

(1 of 6 Flip-Flops)

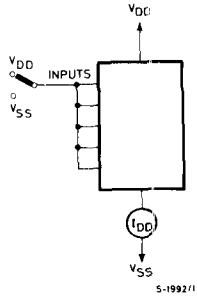


INPUTS			OUTPUT
CLOCK	DATA	$\overline{CLEAR}$	Q
⌐¬	0	1	0
⌐¬	1	1	1
¬⌐	X	1	NC
X	X	0	0

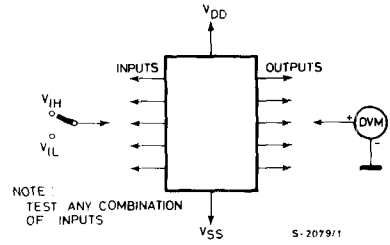
1 = High level
0 = Low level
X = Don't Care
NC = No Change

TEST CIRCUITS

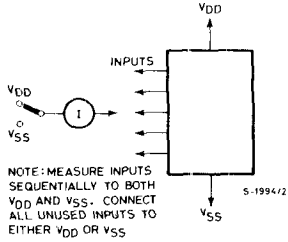
Quiescent device current



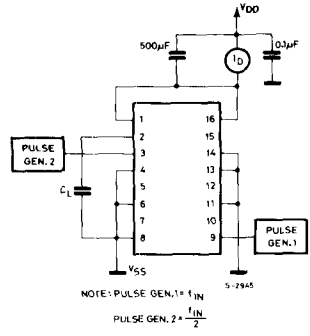
Input voltage



Input leakage current



Dynamic power dissipation



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

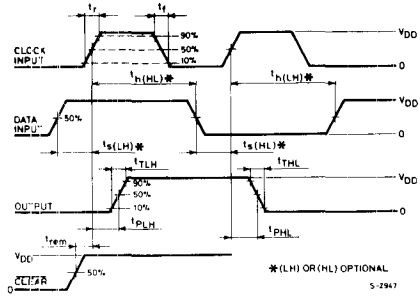
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		±0.1			$\pm 10^{-5}$		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** devices; - 40°C for **HCF** devices.
* T_{High} = +125°C for **HCC** devices; + 85°C for **HCF** devices.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

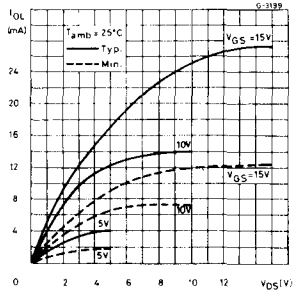
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time Clock to output	5		150	300	ns
		10		70	140	
		15		50	100	
t_{PHL}	Propagation delay time $\overline{\text{Clear}}$ to output	5		100	200	ns
		10		50	100	
		15		40	80	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t_{setup}	Data setup time	5	40	20		ns
		10	20	10		
		15	10	0		
t_{hold}	Data hold time	5	80	40		ns
		10	40	20		
		15	30	15		
t_W	Clock input pulse width Low level	5	130	65		ns
		10	60	30		
		15	40	20		
t_W	Clock input pulse width High level	5	130	65		ns
		10	60	30		
		15	40	20		
t_W	$\overline{\text{Clear}}$ input pulse width Low level	5	100	50		ns
		10	50	25		
		15	40	20		
t_r, t_f	Clock input rise or fall time	5			15	μs
		10			15	
		15			15	
t_{rem}	$\overline{\text{Clear}}$ removal time	5	0	-40		ns
		10	0	-15		
		15	0	-10		
f_{CL}	Maximum clock input frequency	5	3.5	7		MHz
		10	6	12		
		15	8	16		

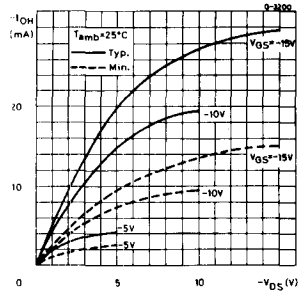
WAVEFORMS



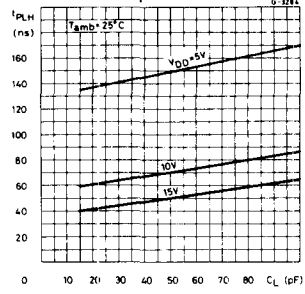
Output low (sink) current characteristics



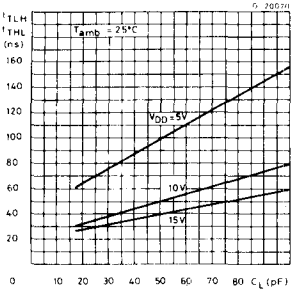
Output high (source) current characteristics



Typical propagation delay time (Clock to output) vs. load capacitance



Typical transition time vs. load capacitance



Typical dynamical power dissipation vs. Clock frequency